CLAIMS

1. A method of reading a digital memory comprising:

receiving, at an output buffer, a first data bit of a data burst from a location at a first electrical distance from said output buffer;

receiving at said output buffer, a second data bit from a second location at a second electrical distance from said output buffer, said second distance larger than said first distance; and

outputting from said buffer said data burst including said first data bit prior to said second data bit.

2. A method of reading a plurality of N data bits of a data burst comprising:

storing said N data bits at respective memory locations in burst order such that a preceding data bits of said burst is electrically closer to a multiplexer than a next subsequent data bit of said burst;

transferring said N data bits to said multiplexer; and,

outputting said N data bits from said multiplexer in burst order.

3. A method of storing a plurality of data bits comprising:

receiving first and second data bit values at first and second memory locations respectively;

transferring said first and second data bit values to first and second multiplexer locations respectively;

completing said transfer of said first bit value from said multiplexer prior to completing said transfer of said second bit value; and

outputting said first bit value from said multiplexer prior to completing transfer of said second bit value.

4. A method of recovering data from a data quadrant of a memory integrated circuit comprising:

receiving a data address from an external address source;

concurrently reading a plurality of bits of data from a respective plurality of memory locations, said locations selected according to said address;

storing said respective plurality of bits in a respective plurality of multiplexer input locations;

outputting said respective plurality of bits from said respective multiplexer input locations in a particular time sequence such that a first bit output is a bit retrieved from one of said plurality of memory locations electrically closest to said respective buffer location.

5. A method of storing data for rapid retrieval comprising:

storing first and second data bits at first and second locations respectively according to a storage rule, said storage rule specifying that a first-to-be-output one of said first and second bits is stored electrically closer to an output buffer than a second-to-be-output one of said first and second bits.

6. A method of reading data from a memory integrated circuit comprising:

receiving an address at an input of an address decoder;

decoding said address within said address decoder;

selecting a plurality of memory storage locations with said address decoder;

receiving a plurality of data bits, one from each location of said plurality of locations respectively;

defining an output order for said plurality of data bits, said output order defining the order of at least first and second data bits such that said first data bit travels a shorter electrical distance between said respective storage location and an output buffer than said second data bit travels between said respective storage location and said output buffer;

sequentially outputting said plurality of data bits in said defined order.

7. A method of outputting data comprising:

storing a first data bit in a first cell at a first location;

storing a second data bit in a second cell at a second location;

said second location being electrically farther from an output buffer than said first location;

said first and second cells adapted to being logically defined by a single address;

receiving said address at an address decoder;

concurrently signaling said first and second cells according to said address; and

outputting said first data bit from said output buffer and subsequently outputting said second data bit from said output buffer.

8. A memory integrated circuit device comprising:

a multiplexer including a plurality of inputs for receiving data, said multiplexer adapted to output data in a particular chronological order such that data received at a first one of said plurality of inputs is output before data received at a last one of said plurality of inputs;

a plurality of memory cells disposed at a respective plurality of different locations; and

a plurality of connecting paths, each paths of said plurality having a characteristic electrical length, each said path switchingly connected between one of said plurality of cells and one of said plurality of multiplexer inputs, the path of said plurality having a shortest electrical length being switchingly connected to said first multiplexer input.

9. A device as in claim 8 further comprising:

an address decoder having an address input adapted to receiving a plurality of encoded address signals;

said address decoder having a plurality of outputs each operatively connected to, and adapted to select, a particular plurality of said cells;

said address decoder adapted to uniquely activate one of said plurality of outputs in response to a unique address signal identifying said plurality.

10. A device as in claim 8 wherein each said connecting path includes traces and devices.

11. An integrated circuit memory storage device comprising:

means for outputting a plurality of bits of data in a particular order such that a first bit of said plurality is output first, said outputting means disposed on an integrated circuit substrate assembly;

means for storing said plurality of data bits including said first bit at a plurality of storage locations disposed on said integrated circuit substrate assembly, one of said storage locations closer than another to said outputting means;

addressing means for receiving a single address signal and responsively transferring said plurality of data bits from said respective plurality of locations to said outputting means, said first bit of said plurality from said closer storage location being said first-output bit.

12. A device as in claim 11 wherein said one closer storage location is the closest storage location of said plurality to said outputting means.

13. A memory integrated circuit device comprising:

an address decoder circuit adapted to receive an address signal;

first and second memory storage circuits adapted to store first and second data values respectively, each said memory storage circuit operatively connected to said address decoder circuit so as to receive from said address decoder circuit a

respective select signal sent concurrently to both said first and second storage circuits; and

a data output circuit operatively connected to said first and second memory storage circuits adapted to receive said first and second data values from said first and second memory storage circuits respectively, said data output circuit adapted to output said respective received data values, said data output circuit being electrically closer to said first memory storage circuit than said second memory storage circuit, said data output circuit adapted to output said first data value from said first memory storage circuit before outputting said second data value from said second memory storage circuit, whereby said first output may occur prior to said receipt of said second data value at said data output circuit.

14. A memory integrated circuit device comprising:

an address decoder circuit;

a memory bank including a first plurality of memory bit storage locations;

a multiplexer including a second plurality of demux bit storage locations, said plurality of demux bit storage locations arranged according to a particular output order, said output order including a first output bit;

a plurality of electrical connections, each including a sense amplifier and a conductive trace, each of said plurality of electrical connections operatively connecting a memory bit storage location of said first plurality to a respective demux storage location of said second plurality, each of said plurality of electrical connections having a characteristic electrical length; and

an electrical connection of said plurality of electrically connections operatively connected to said first output bit having a characteristic electrical length no longer than the characteristic electrical length of any other electrical connection of said plurality of electrical connections.

15. A memory integrated circuit device comprising:

means for receiving a memory address from an external address source;

a plurality of memory bit storage locations, said locations corresponding to said memory address;

means for decoding said memory address;

means for retrieving a plurality of bits of data concurrently from said plurality of memory bit storage locations respectively according to said decoded address;

means for outputting said plurality of bits serially in a particular order such that a first bit output of said plurality is a bit stored at one of said storage locations electrically closer to said outputting means than a subsequent bit of said plurality.

16. A method of storing data to be retrieved and output in a single read cycle of an integrated circuit memory device comprising:

storing a first-to-be-output data value in a first memory cell of said memory device at a first electrical distance from an output buffer of said memory device; and

storing a second-to-be-output data value in a second memory cell of said memory device at a second electrical distance from said output buffer, wherein said second electrical distance is always longer than said first electrical distance.

17. A serial data output signal comprising:

a plurality of data bits forming a data burst, said plurality of data bits including a first-output data bit and a last-output data bit, said first-output data bit representing a value stored in a first memory cell and said last-output data bit representing a value stored in a second memory cell, said first and second memory cells incorporated in a memory device including a multiplexer and located at respective first and second electrical distances from said multiplexer, said first electrical distance being shorter than said second electrical distance.

18. A serial data output signal as a claim 17 wherein said first bit is output from said multiplexer at a time prior to the arrival of said second bit at said multiplexer, both bits being output during a single read cycle of said memory device.

19. A computer processing system comprising:

a central processing unit;

a digital memory operatively connected to said central processing unit by means of a communication bus, said digital memory including an address decoder, a multiplexer, and first and second memory cells at respective first and second electrical distances from said multiplexer, said first electrical distance being shorter than said second electrical distance, said first and second memory cells adapted to store first and second data values respectively, said buffer adapted to receive respective first and second signals corresponding to said first and second data values from said first and second memory cells respectively and to output said first signal to said central processing unit before outputting said second signal, thereby adhering to a fixed burst order.